IN THE CLAIMS:

Please amend claims 1, 11-12, 14-16, 20, 25, 26, 27, 31, 35, 37, 40, 41, and 42 as follows.

1. (Currently Amended) A network switch, said network switch comprising:

at least one data port interface supporting a plurality of data ports;

a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data;

at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit the data between said network switch and other network switches to create a predetermined configuration, wherein the data is removed from said at least one stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed;

~~a CPU interface, said CPU interface configured to communicate with a CPU;~~

a memory management unit in communication with said at least one data port interface and said at least one stack link interface; and

a memory interface in communication with said at least one data port interface and said at least one stack link interface, wherein said memory interface is configured to communicate with a memory~~; and~~,

~~a communication channel, said communication channel for communicating data and messaging information between said at least one data port interface, said at least one stack link interface, said memory interface, and said memory management unit,~~

wherein said memory management unit is configured to route data received from each of said at least one data port interface and said at least one stack link interface to the memory interface.

2. (Original) A network switch as recited in claim 1, wherein said memory interface further comprises:

an internal memory in communication with said at least one data port interface and said at least one stack link interface; and

an external memory interface in communication with said at least one data port interface and said at least one stack link interface, wherein said external memory interface is configured to communicate with an external memory.

3. (Previously Presented) A network switch as recited in claim 1, wherein said bi-directional gigabit stack link interface is configured to interconnect with another bi-directional gigabit stack link interface on a second network switch.

4. (Canceled)

5. (Original) A network switch as recited in claim 1, said network switch further comprising:

a variable sized address resolution logic table; and

a variable sized VLAN table,

wherein said variable sized address resolution logic table and said variable sized VLAN table is in communication with said memory management unit, said at least one stack link interface, and said at least one data port interface.

6. (Original) A network switch as recited in claim 2, wherein said memory management unit directs data to said internal memory and said external memory interface in accordance with a predetermined algorithm, and wherein the configuration of the internal memory and external memory interface results in a distributed hierarchical shared memory configuration.

7. (Original) A network switch as recited in claim 1, wherein said at least one data port interface further comprises:

at least one first data port interface supporting a plurality of first data ports for sending and receiving data at a first data rate; and

at least one second data port interface supporting at least one second data port for sending and receiving data at a second data rate.

8. (Previously Presented) A network switch as recited in claim 7, wherein said at least one first data port interface is an ethernet data port interface and said predetermined

configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration.

9. (Original) A network switch as recited in claim 7, wherein said at least one second data port interface is a gigabit ethernet data port interface.

10. (Original) A network switch as recited in claim 7, wherein one of said at least one second data port interface further comprises a gigabit data port interface configured to interconnect said network switch to another network switch in a stack of switches.

11. (Currently Amended) A network switch as recited in claim 1, wherein said at least one data port interface, said at least one stack link interface, ~~said~~ a CPU interface, said memory interface, said memory management unit, and ~~said~~ a communication channel are integrated on a single application specific integrated circuit (ASIC) chip.

12. (Currently Amended) A network switch as recited in claim 1, wherein said at least one data port interface, said at least one stack link interface, ~~said~~ a CPU interface, said memory interface, said memory management unit, and ~~said~~ a communication channel are configured to perform layer two switching at linespeed.

13. (Canceled)

14. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data;

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed;

~~a CPU interface configured to communicate with a CPU;~~

a memory management unit in communication with said at least one data port interface and said predetermined number of stack link interfaces; and

a memory interface in communication with said at least one data port interface and said predetermined number of stack link interfaces, wherein said memory interface is configured to communicate with a memory~~; and~~

~~a communication channel, said communication channel for communicating data and messaging information between said at least one data port interface, said predetermined number of stack link interfaces, said memory interface, and said memory management unit~~.

15. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and, ~~wherein~~ said predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

16. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a ~~preedetermined~~predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, wherein said at least one data port interface further comprises:

at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate~~;~~, and

at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

17. (Previously Presented) A scalable network switch as recited in claim 16, wherein said at least one first data port interface is an ethernet data port interface supporting a plurality of ethernet data ports and said predetermined configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration.

18. (Original) A scalable network switch as recited in claim 16, wherein said at least one second data port interface is a gigabit ethernet data port interface supporting at least one gigabit data port.

19. (Original) A scalable network switch as recited in claim 18, wherein said gigabit ethernet data port interface supports at least one gigabit ethernet data port configured to interconnect a first building block in a fully meshed cluster of building blocks to at least one other building block across a stack of interconnected building blocks.

20. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, wherein each of said predetermined number of stack link interfaces further comprise a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another switch building block.

21. (Original) A scalable network switch as recited in claim 14, wherein said memory interface further comprises:

an internal memory in communication with said at least one data port interface and said predetermined number of stack link interfaces; and

an external memory interface in communication with said at least one data port interface and said predetermined number of stack link interfaces, said external memory interface being configured to communicate with an external memory,

wherein said internal memory and said external memory interface in communication with an external memory operate to create a shared hierarchal memory configuration.

22. (Previously Presented) A scalable network switch as recited in claim 14, wherein said memory interface is in communication with an external memory and said predetermined configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration.

23. (Original) A scalable network switch as recited in claim 22, wherein said external memory is SRAM.

24. (Canceled)

25. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; and

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, wherein at least one of said predetermined number of switch building blocks further comprises:

~~a CPU interface configured to communicate with a CPU;~~

a memory management unit in communication with said at least one data port interface and said predetermined number of stack link interfaces;

a memory interface in communication with said at least one data port interface and said predetermined number of stack link interfaces, wherein said memory interface is configured to communicate with a memory~~; and~~

~~a communication channel, said communication channel for communicating data and messaging information between said at least one data port interface, said predetermined number of stack link interfaces, said memory interface, and said memory management unit~~.

26. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, ~~wherein~~ said predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

27. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, wherein said at least one data port interface further comprises:

at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate;, and

at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

28. (Original) A scalable network switch as recited in claim 27, wherein said at least one first data port interface is an ethernet data port interface supporting a plurality of ethernet data ports.

29. (Original) A scalable network switch as recited in claim 27, wherein said at least one second data port interface is a gigabit ethernet data port interface supporting at least one gigabit data port.

30. (Original) A scalable network switch as recited in claim 29, wherein said gigabit ethernet data port interface supports at least one gigabit ethernet data port configured to interconnect a first building block in a fully meshed cluster of building blocks to at least one other building block across a stack of interconnected building blocks.

31. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; ~~and~~

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks

to create a predetermined configuration, wherein the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, wherein each of said predetermined number of stack link interfaces further comprise a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another building block.

32. (Original) A scalable network switch as recited in claim 25, wherein said memory interface further comprises:

an internal memory in communication with said at least one data port interface and said predetermined number of stack link interfaces; and

an external memory interface in communication with said at least one data port interface and said predetermined number of stack link interfaces, said external memory interface being configured to communicate with an external memory,

wherein said internal memory and said external memory interface in communication with an external memory operate to create a shared hierarchal memory configuration.

33. (Previously Presented) A scalable network switch as recited in claim 25, wherein said memory interface is in communication with an external memory and said

predetermined configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration.

34. (Original) A scalable network switch as recited in claim 33, wherein said external memory is SRAM.

35. (Currently Amended) A scalable network switch, said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration, wherein at least one of said predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data;

a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data; and

a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a predetermined configuration, said scalable network switch further comprising a physical layer transceiver in connection with at least one of said plurality of data ports, wherein the data is removed from said predetermined number of stack link interfaces in a

reverse order from that in which the data is added, where the most recently added data is the first one removed.

36. (Canceled)

37. (Currently Amended) A method of stacking network switches, said method comprising ~~the steps of~~:

providing a plurality of clustered switch blocks; and

interconnecting each one of said plurality of clustered switch blocks to another one of said plurality of clustered switch blocks,

wherein interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks, wherein the ~~step of~~ providing ~~a~~ of the plurality of clustered switch blocks further comprises ~~the steps of:~~

providing a predetermined number of switch building blocks;

interconnecting each of said predetermined number of switch building blocks to every other one of said predetermined number of switch building blocks in a meshed configuration; ~~and~~

adding an interstack tag into data received to keep track of a stack count to prevent looping of the data,

wherein each of said predetermined number of switch building blocks is interconnected to every other one of said predetermined number of switch blocks through an individual stack link; and

removing the data from said individual stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

38. (Original) A method for stacking network switches as recited in claim 37, wherein a number of stack links required for each switch building block is one less than an actual number of the predetermined switch building blocks.

39. (Canceled)

40. (Currently Amended) A method of stacking network switches, said method comprising ~~the steps of~~:

providing a plurality of clustered switch blocks; and

interconnecting each one of said plurality of clustered switch blocks to another one of said plurality of clustered switch blocks,

wherein interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks~~, wherein said receiving step further comprises the steps of:~~;

receiving a packet on at least one of a data port interface and a stack link interface~~;~~;

adding an interstack tag into the packet to keep track of a stack count to prevent looping of the packet, and

storing the packet in a memory in accordance with a predetermined algorithm by allocating memory locations in an internal memory and in an external memory based upon an amount of internal memory available for an egress port of the clustered network switch from which the packet is to be transmitted; and

removing the data from said stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

41. (Currently Amended) A method of stacking network switches, said method comprising ~~the steps of~~:

providing a plurality of clustered switch blocks; and

interconnecting each one of said plurality of clustered switch blocks to another one of said plurality of clustered switch blocks,

wherein interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks~~, wherein said forwarding step further comprises the steps of:~~;

receiving a packet~~;~~;

adding an interstack tag into the packet to keep track of a stack count to prevent looping of the packet~~;~~;

determining if the destination address of the packet corresponds to a port in the clustered network switch;

forwarding the packet to the port corresponding to the destination address if the destination address is determined to correspond to a port in the clustered network switch;

determining if the destination address of the packet corresponds to a port on another clustered network switch across a stack;

forwarding the packet to a stack link if the destination address is determined to correspond to a port on said another clustered network switch across the stack; ~~and~~

removing the data from said stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed; and

transmitting the packet across the stack to said another clustered network switch if the destination address of the packet corresponds to a port on said another clustered network switch across the stack.

42. (Currently Amended) A method of stacking network switches as recited in claim 41, wherein said ~~step of~~ determining if the destination address of the packet corresponds to a port on another clustered network switch across a stack further comprises using the interstack tag.